First Quarterly Report

for

Development of Multiple Source - Multiple Low Voltage Converter-Regulator Power Supply with Automatic Failure Sensing and Redundant Switching

(30 June 1966 - 30 September 1966)

Contract No. NAS 5-10148

Prepared by

Honeywell Inc.
Ordnance Division
Hopkins, Minnesota

for

Goddard Space Flight Center
Greenbelt, Maryland

DEVELOPMENT OF MULTIPLE SOURCE - MULTIPLE LOW VOLTAGE CONVERTER-REGULATOR POWER SUPPLY WITH AUTOMATIC FAILURE SENSING AND REDUNDANT SWITCHING

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SUMMARY

This report describes the technical details of the work performed during the first quarter of Contract NAS 5-10148. The object of this contract is to develop technologies and a model which will demonstrate the feasibility of achieving high efficiency, high reliability low input voltage converter-regulator (LIVCR) systems by combining proven LIVCR configurations with newly developed techniques in the general area of automatic failure sensing and compensation. The feasibility of other techniques to achieve high reliability will also be investigated and reported, included among which will be circuits to provide overvoltage protection for thermoelectric generators and methods for charging third electrode batteries with an LIVCR. The LIVCR model, which will be built to verify the technologies developed from the researches conducted during this contract, will be delivered to NASA-GSFC at the termination of the contract.

Technical work during the first quarter was directed toward completion of the initial phases of three major tasks. The first task involved the design, development, and initial testing of a pulse width modulated (PWM) regulator drive and control circuit with automatic failure sensing and compensation features. (Failure compensation for this circuit is defined as the removal of a failed circuit from the system and its replacement with an operational circuit.) Combining the technical characteristics of the EXG2511A1X1 LIVCRs delivered to GSFC under Contract NAS 5-9212 and new techniques of sensing and compensating for failures, the breadboard circuits thus far tested have proved the feasibility of automatically sensing failures and replacing system functions which have failed with functions that are operational. Numerous failures were simulated in various redundant portions of the tested circuit; in every case the new failure sensing and compensation circuits successfully returned the system to an operational condition. The tests imply that, by carefully selecting those portions of the system to be

duplicated, the incorporation of automatic failure sensing and compensation features will ensure a significant increase in useful system life.

The second major task involved the design, fabrication, and initial testing of two alternative circuits for synchronizing four redundant LIVCs. The advantage of synchronization would eliminate the frequency beating between LIVCs which is characteristic of non-synchronous operation. In addition to synchronization, and the chief way in which the two alternative methods differ, is the phase relationships under which the LIVCs operate. One method, which proved highly efficient in tests and which is therefore preferred, involves the phase separation of each of the four LIVCs by 45 degrees. The alternative method, with which a number of difficulties were experienced and which is therefore not recommended, involves the phase separation of each of three LIVCs by 120 degrees, with a fourth LIVC in phase with one of the other three. Phase separation, as has been proved during previous contracts, notably NAS 5-9212, significantly reduces the input and output transients caused by the switching of LIVC oscillators, with a consequent decrease in overall system power consumption. Moreover, the synchronization techniques perfected during previous contracts enables phase-separated synchronization after failures, a feature which was proved again with four LIVCs during the tests conducted during this quarter, in which the synchronized, phase-separated LIVC system continued to function efficiently with only 50 percent of the original system (two LIVCs) still operational. Phase-separated synchronization of the type investigated this quarter appears to be highly applicable to power conditioning systems with high power and reliability requirements.

The third major task involved the design, fabrication, and testing of a circuit for decreasing half-cycle unbalance in the current feedback transformers. The circuit developed during this quarter will not solve, in itself, the half-cycle unbalance problem. Rather, the circuit is intended to

complement matched oscillator transistors and cores with high reset properties. Indeed, tests indicate that, other than mismatched transistors and unbalanced cores, half-cycle unbalance can result from temperature changes, component aging, and system exposure to nuclear radiation. Since the circuit developed and tested during this quarter will compensate for the degree of half-cycle unbalance that could be normally expected to result from environmental changes, it is recommended that this circuit be considered, along with matched oscillator transistors and high reset cores, for use in long-duration space missions and similar applications where long-term changes in components due to extended exposure to severe environments can be expected. Since the circuit developed is relatively complex, this factor should be weighed carefully against the weight, space, and reliability requirements of a given application, to determine the relative usefulness of such a circuit in any given LIVCR system. Such a trade-off would apply especially to LIVCR systems designed for experiments in space.

I. ACTIVITIES OF THE FIRST QUARTER

A. INTRODUCTION

This report describes the technical research, development, and tests performed during the first quarter of Contract NAS 5-10148, "Development of Multiple Source - Multiple Low Voltage Converter-Regulator Power Supply with Automatic Failure Sensing and Redundant Switching". This program is a continuation and amplification of work completed under Contract NAS 5-9212. The purpose of this program is the development of technologies for providing highly reliable LIVCR systems for space applications. The following are major areas of work required to define these technologies:

1) The development of automatic failure sensing and compensation circuitry for the LIVC sections, PWM regulator power sections, and PWM regulator drive and control section of the redundant LIVCR.

2) The development of circuitry to establish phase separated synchronization of redundant LIVCs.

3) The investigation of techniques to eliminate half-cycle unbalance in the LIVC power oscillator and to generally improve LIVC performance.

4) An investigation of the feasibility of charging third electrode batteries with the basic LIVCR.

5) The development and study of circuitry to provide overvoltage protection for thermoelectric generators.

The technologies developed during this program will be applied to the fabrication of a 375-watt, breadboard-type LIVCR model for operation from a thermoelectric generator. The LIVCR model will be delivered to NASA-GFSC upon program completion.

The following tasks, the technical aspects of which are described in detail in this report, were completed during the first quarter:

1) The design, fabrication, and initial testing of a PWM regulator drive and control circuit with automatic failure sensing and compensation features.

2) The design, fabrication, and initial testing of two alternative circuits for synchronizing four redundant LIVCs.

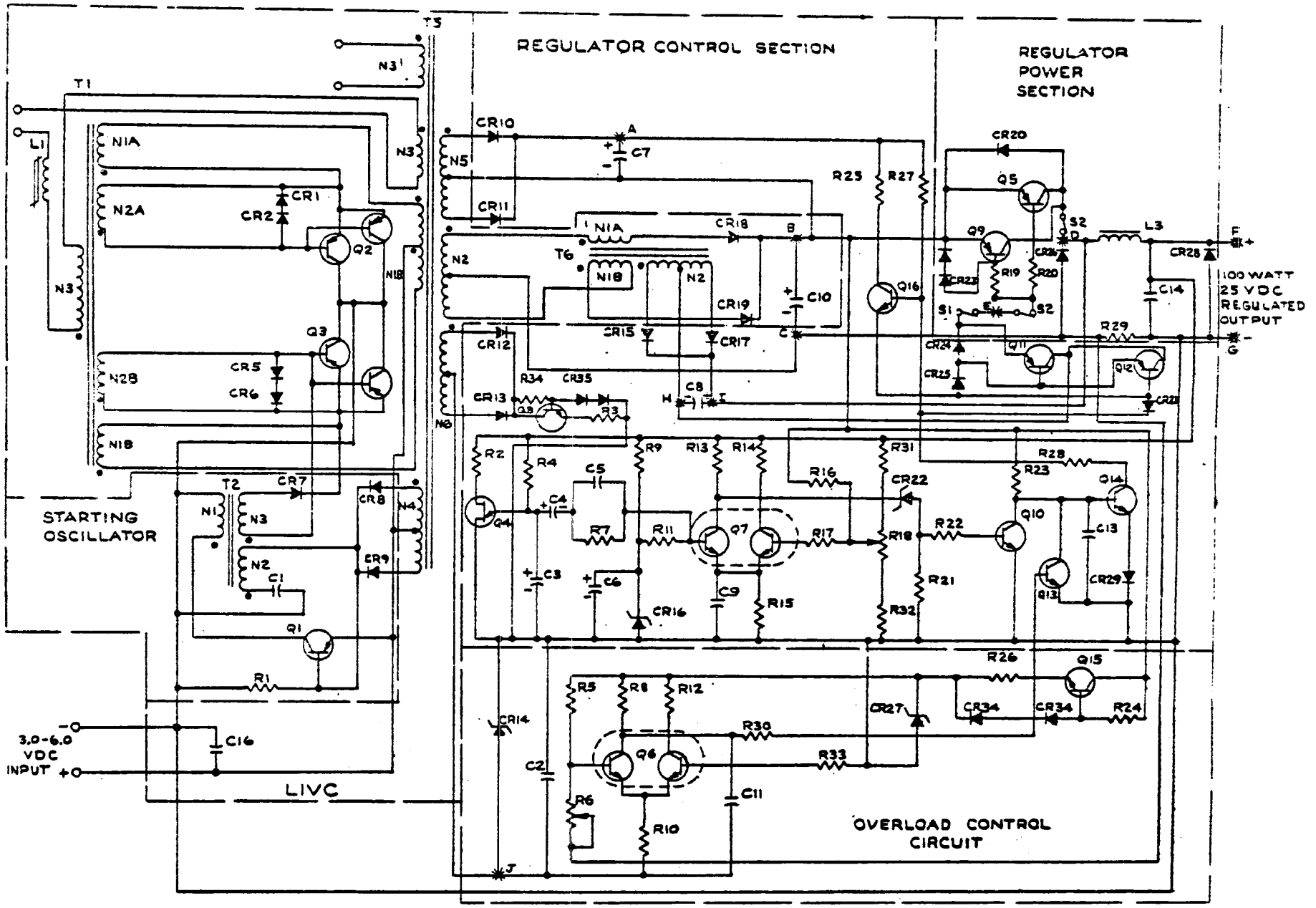
3) The design, fabrication, and initial testing of a circuit for decreasing half-cycle unbalance in the current feedback transformers.

B. TECHNICAL DISCUSSION

1. PWM Regulator Drive and Control with Automatic Failure Sensing and Compensation

The method of automatic failure sensing and compensation for the redundant LIVCR being developed under this contract is based on similar (but manual) circuitry incorporated in the EXG 2511A1X1 LIVCRs delivered under Contract NAS 5-9212. (A circuit diagram for LIVCR EXG 2511A1X1 is shown in Figure 1). As shown in Figure 1, drive and control circuits for the Pulse Width Modulator (PWM) regulator incorporate standby redundancy; that is, only one of the redundant circuits operates at any one time. An "on-off" toggle switch (S1 in Figure 1) was provided on each EXG 2511A1X1 for manually selecting (either connecting or isolating) redundant drive and control circuits.

The work this quarter included the design and fabrication of transistor circuitry for automatically performing the functions which are performed manually with the S1 switches in the redundant LIVCR delivered under NAS 5-9212. The overload control circuitry was not included in the failure mode simulation considered for the automatic failure sensing and compensation circuitry design, but can be included in future work.



* SYMBOL INDICATES COMMON POINTS

Figure 1 - LIVCR EXG2511A1X1, CIRCUIT DIAGRAM

Operational tests indicated that the automatic failure sensing and compensation desired in the PWM drive and control circuit have been provided. The design, development and operation of this circuit are discussed in the following paragraphs. Specific components for accomplishing the desired function could probably be different than those selected. Of greatest significance is the basic design which was chosen, the testing of which indicated that the performance sensing functions, the logic sequence, and the switching techniques are valid and effective for achieving the functions desired. The design approach used lends itself to fabrication with integrated circuit blocks, a method which would be very desirable for space applications in which size, weight and reliability requirements are critical.

a. Definition of Failure - In regards to the performance of the PWM drive and control circuit, circuit failure is defined as system performance below an acceptable level caused by any component change in any circuit. Circuit failures could be quite accurately analyzed automatically by monitoring the performance of each component in the circuit, but such a monitoring system is too complex to be practicable. A more easily implemented approach, and one which is widely used, involves monitoring various circuit performance characteristics or combinations of characteristics to determine when certain functions have degraded to a level where replacement by redundant functions is necessary. This is the approach used in the circuitry developed this quarter. Drive current, regulator output voltage, and the conditions of all redundant drive and control circuits are monitored. The drive and control circuits are the redundant functional elements subject to replacement.

A failure in a drive and control circuit is indicated when:

1) The regulator output voltage is too high and drive current is supplied to the regulating transistor, or when

2) The regulator output voltage is too low and no drive current is supplied to the regulating transistor.

These two combinations of circuit characteristics are the only failures which can be attributed to malfunctions of the drive and control circuit. If such a failure is indicated, the failed circuit should be isolated and replaced by an operational circuit.

While not part of the failure definition, the conditions of all regulator drive and control circuits should be monitored and included in the logic sequence for circuit implementation, to ensure positive transition to a new circuit on command.

b. Failure Sensing and Compensation - The failure definition stated in paragraph 1. a was the basis for designing the operational automatic failure sensing and compensating circuitry for the PWM regulator drive and control circuit (see Figure 2). Conventional and zener diodes are used as the primary sense elements. Transistor Q4, which replaces the functions of toggle switch S1 in Figure 1, automatically connects or isolates the associated drive and control circuit. While the design approach was implemented for a redundant combination of only two circuits, redundancy could be increased to three circuits without difficulty.

The circuit diagram of Figure 2 indicates the interconnection between one PWM regulator power section, two PWM drive and control sections, and two automatic failure sensing and compensation sections.

The PWM power section and drive and control sections are shown only in enough detail to indicate the general operation with the sense and compensation circuitry. Note that the two sense and compensation circuits are identical. Also, the indicated ground reference is common with the regulator output ground. The following paragraphs describe the functions of one sense and compensation circuit.

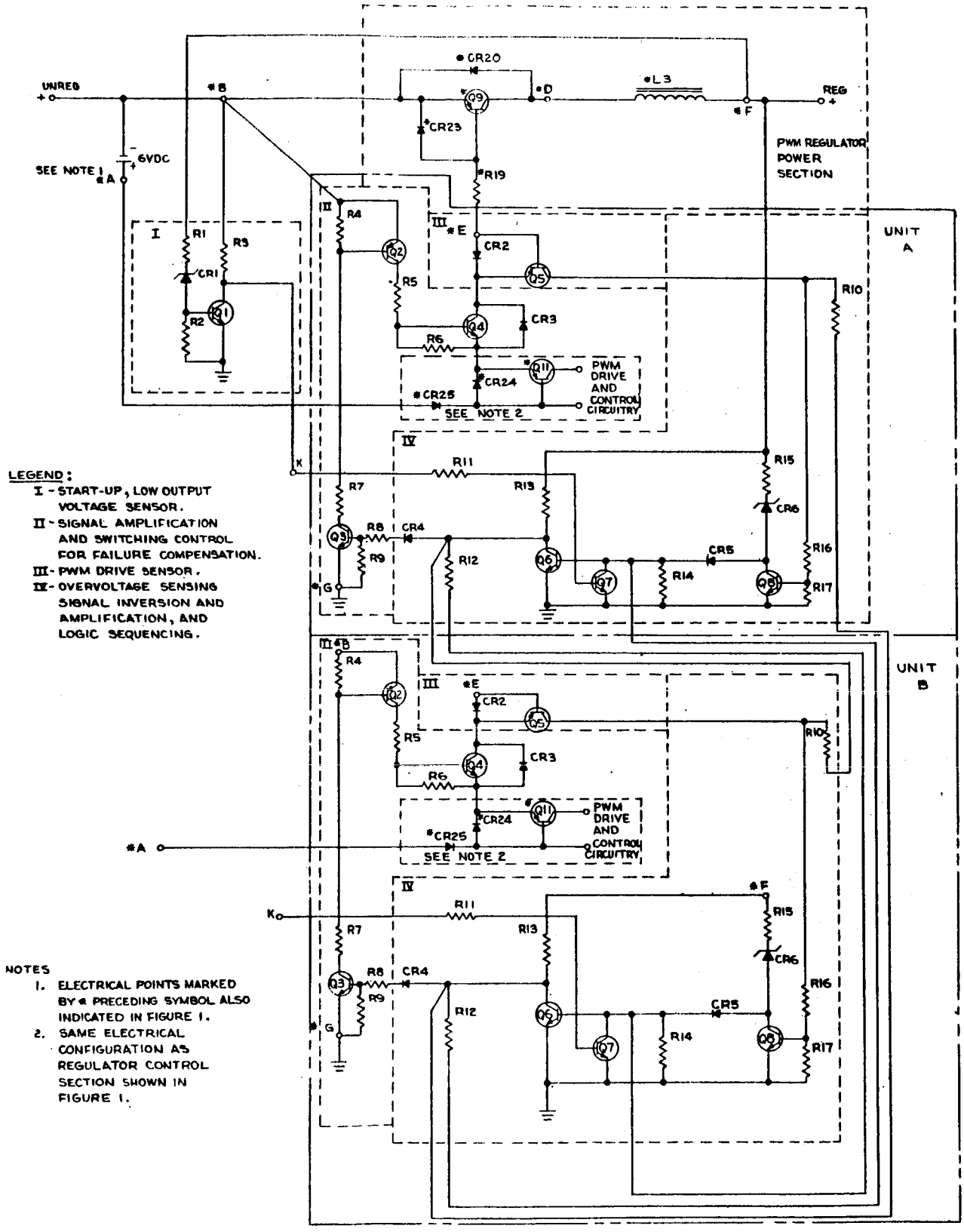


Figure 2 - PWM REGULATOR DRIVE AND CONTROL WITH AUTOMATIC FAILURE SENSING AND COMPENSATION

Transistor Q4, which replaces the functions of S1 in Figure 1, is the component around which the failure compensation circuit is designed. The transistor is driven fully "on" (saturation) or held "off" (no drive) to provide the necessary "on-off" function. Only one Q4 is "on" in any redundant combination. Diode CR3 does not interfere with the switching action of the PWM drive current because the drive current flow and the diode are unidirectional and connected in opposition to one another. (CR3 provides the path for turn-off current to the PWM regulating transistor Q9.) The reliability of Q4 must be very high (several times greater than the circuit which it switches) to achieve the overall reliability desired in the redundant system. Reliability of the required level will be ensured by specifying Q4 to strict requirements and by operating Q4 well below the rated capacity.

A low PWM regulator output voltage is indicated through Block I (see Figure 2). If the output voltage is below that necessary for CR1 to conduct, Q1 remains off. With Q1 off, a positive voltage is provided at the collector of Q1 through R3. This signal is also used to initiate operation during start-up.

The circuits in Block III sense whether drive current is being supplied to the PWM regulating transistor Q9. If drive current is being supplied, it must flow through CR2 and clamp Q5 off. If drive current is not supplied, Q5 conducts (obtaining power from the PWM turn-off circuit), thus providing a positive voltage at its own collector. The drive current is sensed most effectively at this point; an alternative point (such as in series with Q14 in Figure 1) would not enable the sensing of all possible failure modes.

Overvoltage sensing, signal inversion and amplification, and logic sequencing is provided by the circuits in Block IV. A high PWM output voltage is indicated when CR6 conducts. A positive signal, sufficient to cause CR5 to conduct, appears at the collector of Q8 unless PWM drive current is not being supplied. Q6 conducts when CR5 conducts or when a signal is introduced through R12 in the redundant Block IV, except when Q7 is conducting

because of a low PWM output voltage. If Q6 does not conduct, a positive voltage appears at the cathode of CR4.

Signal amplification and switching control for failure compensation is provided by the circuits in Block II. Q3 conducts if a positive voltage exists at the cathode of CR4. If Q3 conducts, Q2 conducts and provides drive for Q4, turning Q4 "on". Q4 is "off" unless Q3 conducts. The switching of Q4 is not of a destructive nature (as is the case of a fuse or squib switch); therefore, if a failure is corrected in a particular circuit, Q4 will be utilized again to reconnect the circuit to the system.

Two possible failure modes in the drive and control circuit and their correction are described as follows:

Case I - Assume that circuit A is operating and Q11 fails shorted. The PWM output voltage rises and drive current is being supplied. Therefore, in Unit A:

1) Q8 is off,
2) CR6 conducts causing Q6 to conduct,
3) Conduction of Q6 turns Q3 off,
4) Q4 is off whenever Q3 is off,
5) Q3 is latched off (a consequence of the action in Unit B (see Step 6),

in Unit B:

1) Q8 is on,
2) CR6 conducts, but CR5 does not conduct because Q8 is on
3) Q6 does not conduct,

4) Q3 conducts because Q6 is off,

5) Conduction of Q3 causes Q2 and Q4 to conduct,

6) Q6 in Unit A is latched on by current flow through R12.

Case II - Assume that circuit A is operating and Q11 fails open. PWM output voltage falls and drive current is not provided. Therefore, in Unit A:

1) Q5 is on,

2) Q7 is on,

3) Q3 is latched off (a consequence of the action in Unit B (see Step 4),

4) Q4 is off when Q3 is off.

in Unit B:

1) Q7 is on,

2) Q3 is turned on by current flow through R10 in Unit A, providing positive voltage at the cathode of CR4,

3) Conduction of Q3 causes Q2 and Q4 to conduct,

4) Q6 in Unit A is latched on by current flow through R12.

The basic circuit has been proven by laboratory testing. A large number of component failures were simulated. In every case, the failure was properly sensed and compensated by the automatic functions in the redundant combinations.

2. Synchronization of Redundant LIVCs

The synchronization of redundant LIVCs was investigated initially by Honeywell under Contract NAS 5-9212. Under that contract, two synchronization circuits, each providing phase separation, were developed, one circuit for operation

with two redundant LIVCs[1] and one for operation with three redundant LIVCs[2] Synchronization eliminates any low frequency ripple which may otherwise be generated by the "beating" of non-synchronized LIVCs. Phase separated synchronization provides the added advantage of reduced input and output transients by separating the switching operations of individual LIVC power oscillators. (While LIVC synchronization is specified, the synchronization actually controls the current feedback oscillator in each LIVC.)

The practical limit on the number of LIVCs which could be redundantly connected, and therefore the synchronization technology required, is determined primarily by the power level and reliability requirements of specific applications. Since LIVC redundant combinations in future space applications may well involve more than three LIVCs, further development and refinement of the synchronization technology were investigated this quarter. The development of two circuits to synchronize four LIVCs is discussed in the following paragraphs.

The general design guidelines for developing synchronization circuitry for four LIVCs are essentially the same as the guidelines for developing a synchronizer for three LIVCs, which are:

1) The synchronization frequency should be directly proportional to the LIVC input voltage.

2) Switching of individual LIVCs should be phase separated to reduce input and output line transients.

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[1] "Second Quarterly Report for a Program of Research and Development of Low Input Voltage Conversion and Regulation", NAS-5-9212, prepared by J. T. Lingle and K. J. Jenson.

[2] "Third Quarterly Report for a Program of Research and Development of Low Input Voltage Conversion and Regulation", NAS-5-9212, prepared by J. T. Lingle and K. J. Jenson.

3) Synchronization should be reliably established upon starting the LIVCs; ideally, starting and synchronization of all LIVCs should be established by pulsing any LIVC.

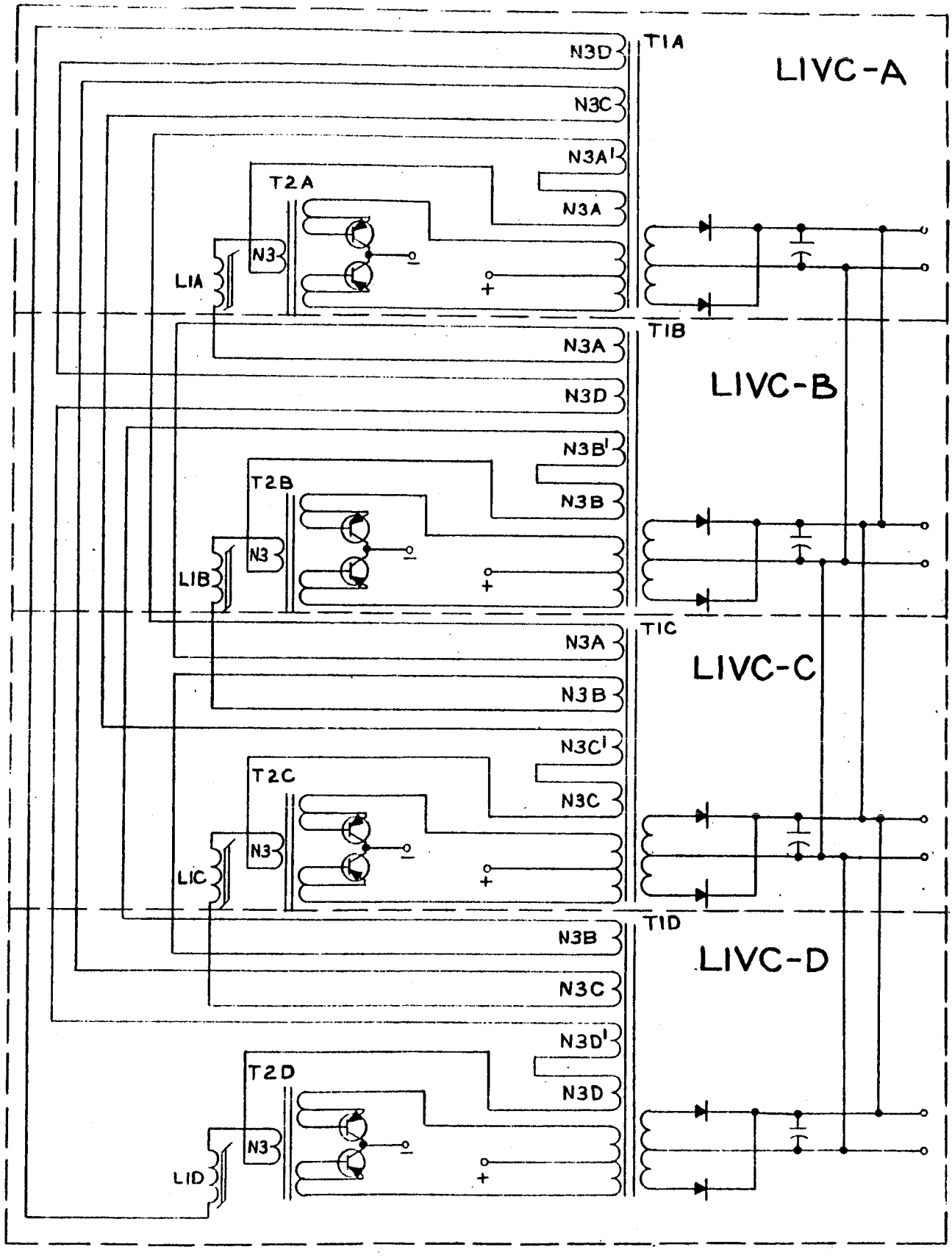
4) The synchronization circuit must not cause the failure of one LIVC to adversely affect an operational LIVC.

5) If any LIVC fails, the operational LIVCs remaining should be synchronized (ideally with phase separation) at approximately the same frequency for an equal input voltage as before the failure. If a frequency change is significant, it should be toward a higher frequency rather than toward a lower frequency.

6) The voltage applied to any frequency controlling inductor should go to zero or reverse immediately after the switching initiated by its saturation is completed.

Although these guidelines are not changed when increasing the number of synchronized LIVCs, the considerations for achieving a design within these guidelines are greater. For example, several voltage summations for the switching inductors which initially appeared adequate for sustained operation did not permit smooth and reliable synchronization after starting. The circuit discussed in section I. C. 2. a erforms efficiently within the design guidelines stated. The circuit discussed in section I. C. 2. b.will require additional design work before it is completely suitable.

a. Synchronization of Four LIVCs with Phase Separation of 45 Degrees - The circuit shown in Figure 3 synchronizes four LIVC current feedback oscillators at a phase separation of 45 degrees. Control is achieved by summing phase voltages from various combinations of three of the four power transformers and applying these voltages to the proper switching inductors (L1A, L1B, L1C and L1D in Figure 3). Each switching inductor has a square loop core. Upon saturation of the core, a current pulse is allowed to flow, in series, through the inductor and the associated current feedback transformer (T2A, T2B, T2C or T2D) winding N3. The current pulse through winding N3 switches the associated LIVC oscillator. Phase



Gigure 3 - SYNCHRONIZER FOR FOUR LIVCs (45° PHASE SEPARATIONS)

summation causes the saturation of inductors and the switching of oscillators to occur at a synchronized, phase separated rate. This design approach is similar to that used to synchronize three LIVCs. The primary difference in the two approaches is the number and phase summation of power transformer voltages applied to each inductor. Each approach is intended for application where LIVC input voltages are approximately equal.

Normal synchronization waveforms are shown inFigure 4. Waveforms A, B, C and D are volts per turn representatives of the voltages on the power transformers of LIVCs A, B, C and D, respectively. The voltage summation 2A-B-C is applied to the switching inductor for LIVC A (L1A), 2B-C-D is applied to L1B, 2C-D+A is applied to L1C, and 2D+A+B is applied to L1D. The area under the 2A-B-C waveform between t = 2 and t = 4 represents the volt-second integral of L1A. Inductor L1A saturates at t = 4, 8, 12, etc., thereby switching LIVC A at those times. Similarly, the redundant LIVCs B, C and D are switched at the times indicated in Figure 4 as a result of the saturation of associated switching inductors. Note that the voltages applied to each inductor goes to zero after the switching operation initiated by saturation is complete. When the applied inductor voltage next deviates from zero, it is in a polarity opposite to that which caused the previous saturation. This characteristic of the inductor voltage enables the synchronization circuitry to operate very efficiently.

The volts per turn on an LIVC power transformer is proportional to the LIVC input voltage. The voltage applied to the switching inductor(s) is also proportional to the LIVC input voltage. Thus, the time required to saturate the inductors varies in an inverse proportion to the LIVC input voltage, while the synchronization frequency is directly proportional to the LIVC input voltage.

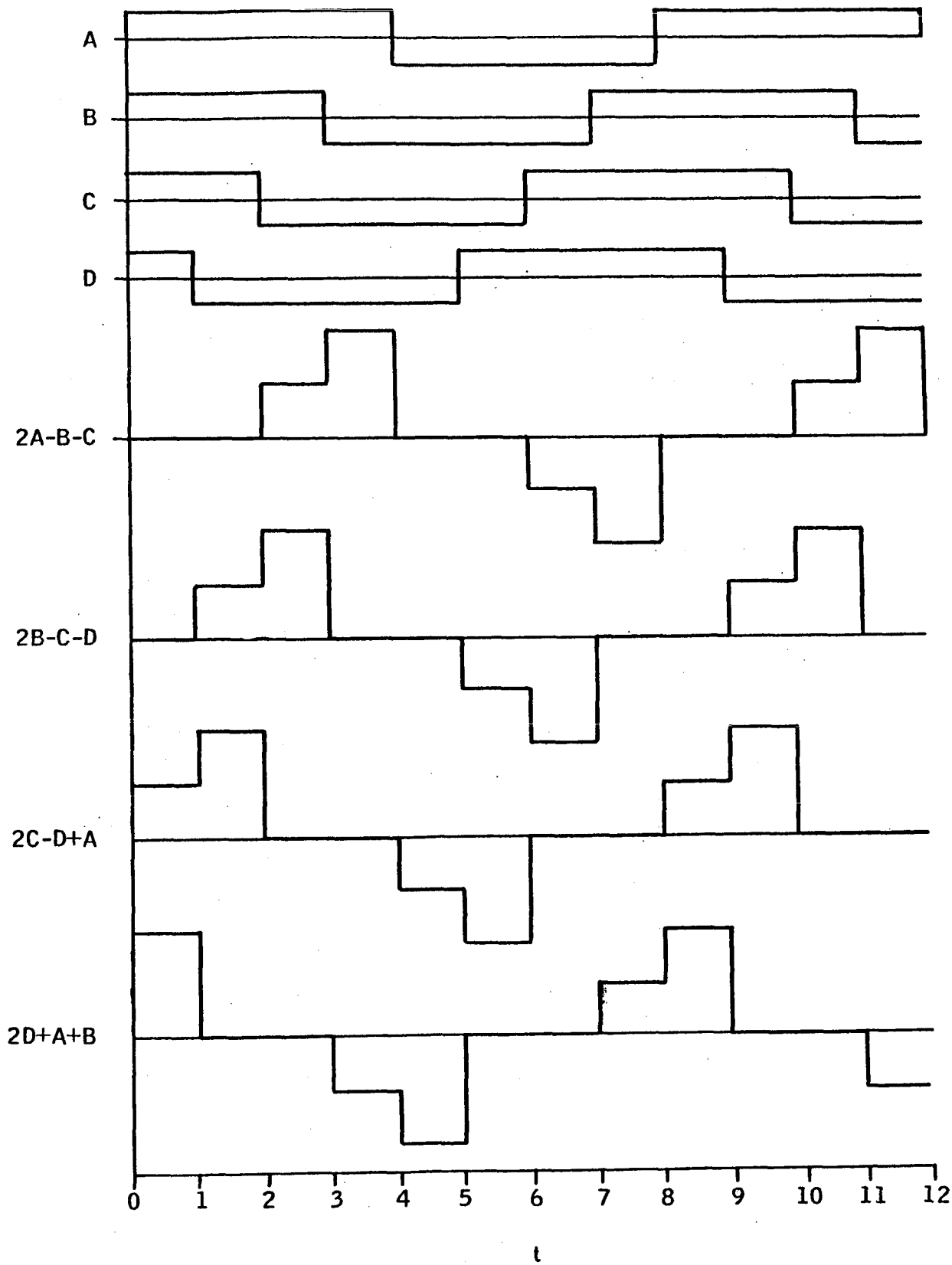


Figure 4 - SYNCHRONIZATION WAVEFORMS (FOUR LIVCs, 45° PHASE SEPARATIONS)

Phase separation is maintained because of the dependence of phase voltage summation on LIVC phase separation, the coupling loops between LIVCs, and the stable operation relationship effected by the summation and coupling.

Starting and phase separated synchronization can be established by pulsing any one of the four redundant LIVCs. If starting pulses are applied to all LIVCs simultaneously, or even in a random manner, the desired normal operation is immediately established.

Failure of one of the four redundant LIVCs results in the waveforms shown in Figure 5. These waveforms, which resulted from input voltages identical to those which produced the waveforms shown in Figure 4, have the following significant characteristics:

1) The operating frequency is approximately 25% greater than the frequency measured when four LIVCs were operational.

2) Phase separated synchronization has been maintained.

3) The volt-second integral applied to the switching inductor of the failed unit is less than that necessary for saturation; therefore, the inductor in the failed unit does not load the operational units.

Failure of two of the four redundant LIVCs results in the waveforms shown in Figure 6. The system is still maintained above the acceptable efficiency level because:

1) The operating frequency is approximately 33 percent greater than the frequency measured when four LIVCs were operational.

2) Phase separated synchronization has been maintained.

3) The inductors in the failed units do not load the operational units.

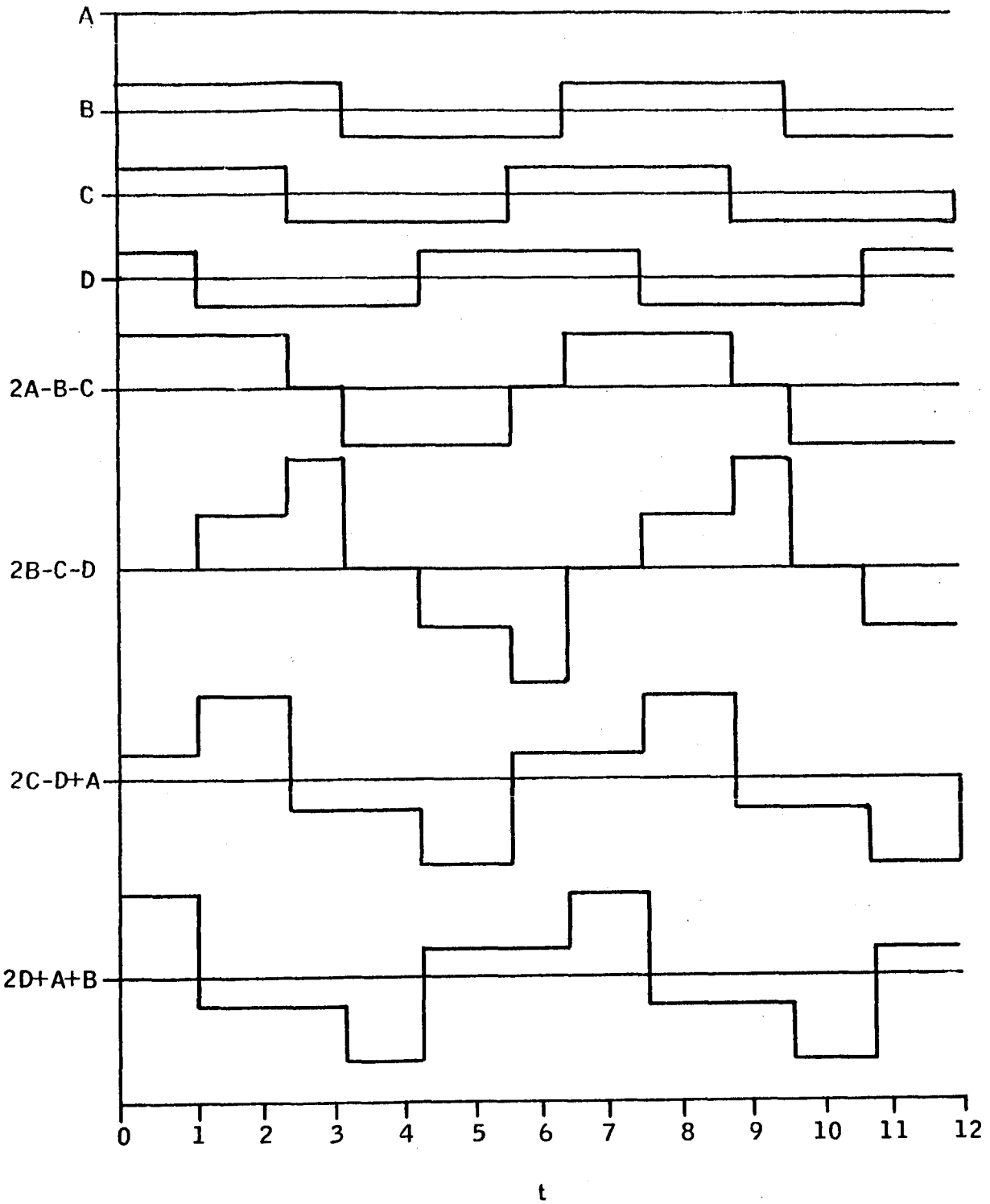


Figure 5 - SYNCHRONIZATION WAVEFORMS AFTER FAILURE OF LIVC A (SEE FIGURE 3)

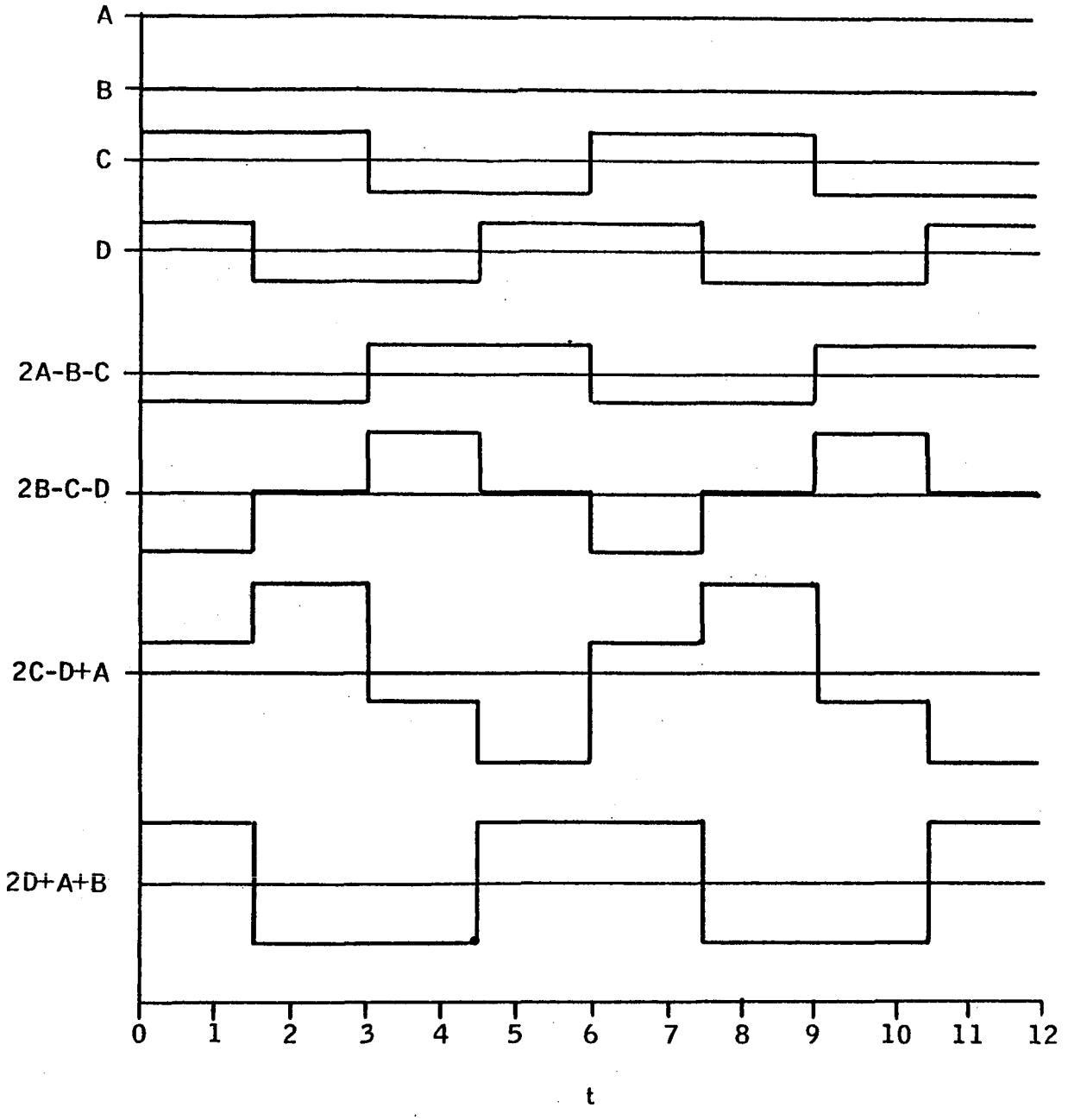


Figure 6 - SYNCHRONIZATION WAVEFORMS AFTER FAILURE OF LIVC A AND LIVC B (SEE FIGURE 3)

Failure of three of the four redundant LIVCs will still enable the operational LIVC remaining to supply its full rated power to the load without performance degradation. The operating frequency would be approximately the same as when two LIVCs were operating.

Laboratory tests of the breadboard of the synchronization circuit shown in Figure 3 verified the performance characteristics stated in the preceding paragraphs.

b. Synchronization of Four LIVCs with Phase Separations of 120 Degrees and 0 Degree - The circuit shown in Figure 7 could be used to synchronize four LIVC current feedback oscillators. Three of the four LIVCs are maintained at a phase separation of 120 degrees; the fourth LIVC operates in phase with the third LIVC. This approach is very similar to the approach described in Section I.C.2.a, except that 1) only three rather than four switching inductors are used, and 2) power transformer phase voltages are summed in a different manner. The saturation of switching inductor L1A causes unit A to switch, the saturation of L1B causes unit B to switch, and the saturation of L1C causes unit C and unit D to switch. Figure 8 shows the normal waveforms for the circuit of Figure 7. The voltage summation $2A + \frac{C}{2} + \frac{D}{2}$ is applied to L1A, 2B+A is applied to L1B, and C+D+B is applied to L1C. Note that a 120-degree phase separation is characteristic between units A, B and C; unit C is in phase with unit D.

While the smooth, normal operation indicated in Figure 8 was verified during laboratory testing, definite problems did exist in starting and establishing these operating conditions. When a starting pulse was applied to one LIVC, it was common for only two of the four LIVCs to start; also, the operating units appeared to be loaded by the non-operational units. This type of operation, which is unacceptable, would have to be eliminated before the circuit operation could be validated. Additional problems were noted when failures were simulated in individual LIVCs. Neither of these two problems

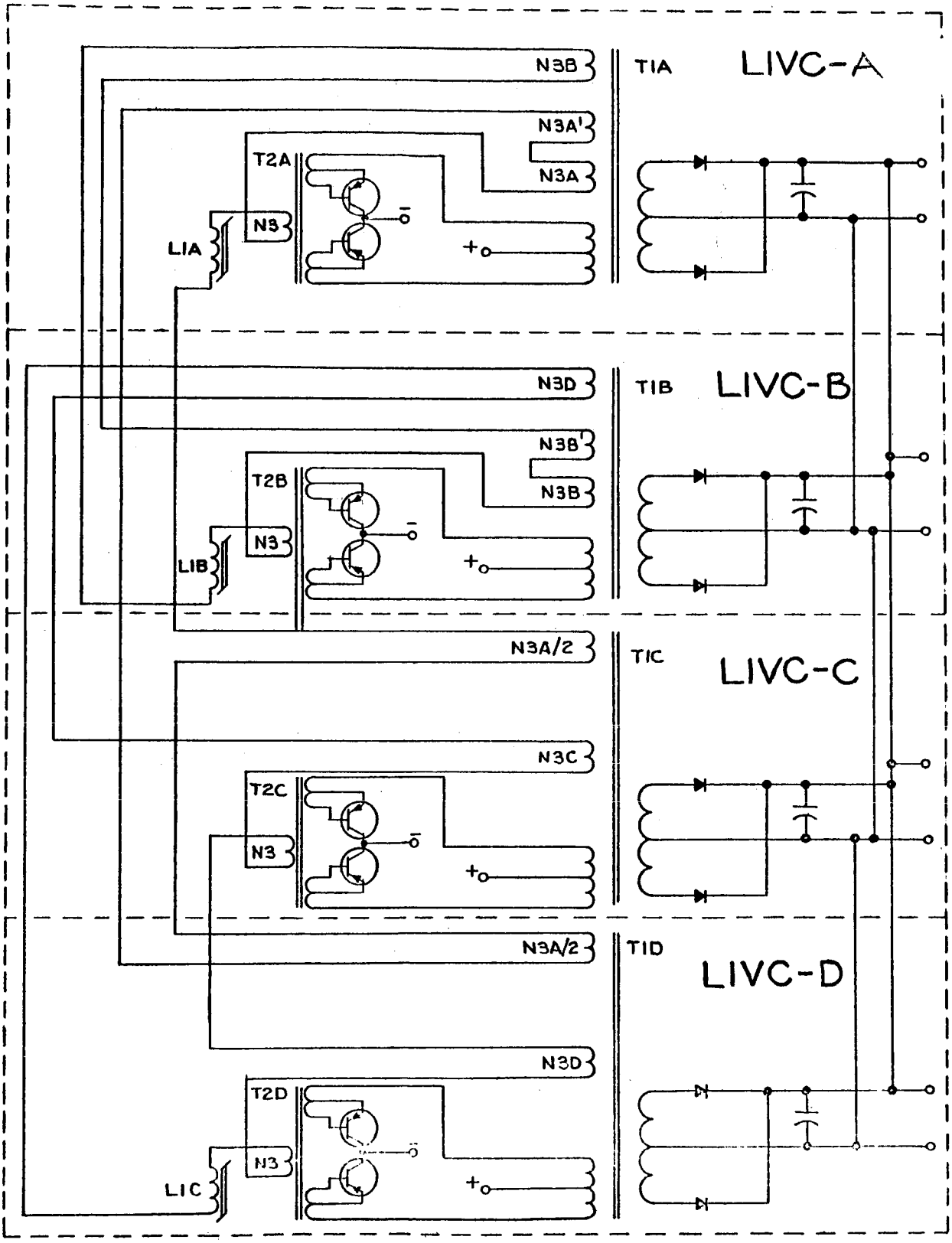


Figure 7 - SYNCHRONIZER FOR FOUR LIVCs (120° AND 0° PHASE SEPARATIONS)

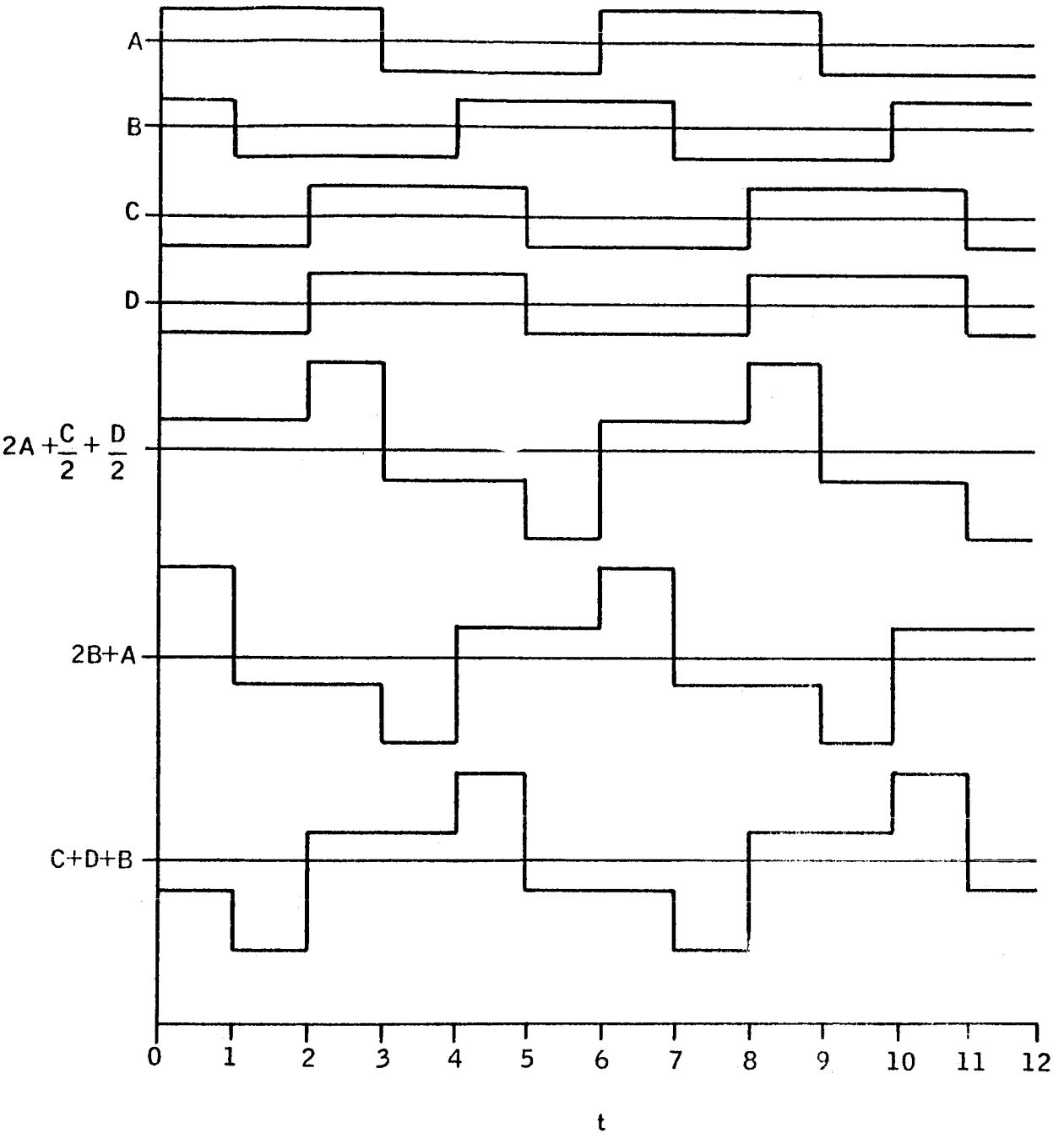


Figure 8 - SYNCHRONIZATION WAVEFORMS (FOUR LIVCs, 120° AND 0° PHASE SEPARATIONS)

were investigated extensively because the circuit of Figure 3 indicated a basic superiority. While the alternative approach may prove to be advantageous and merit additional work in the future, present plans are concerned with further study and refinement of the approach represented by the circuit shown in Figure 3.

3. Decreasing Unbalance in the LIVC Current Feedback Transformer

A circuit to decrease unbalance in the LIVC current feedback transformer was designed and tested this quarter with favorable results. The design approach involved equalizing the volts per turn on the current feedback transformer during succeeding half-cycles by varying the power transistor drive current on each half-cycle as a function of any mismatch in their respective emitter-base characteristics. The varied drive current controls the respective junction resistive voltage drop which, in turn, is a significant percentage of the total junction voltage which determines the resulting volts per turn on the current feedback transformer. This approach, which results in a design which functions efficiently, is meant to complement matched power transistors and transformer cores with a low squareness ratio (B_R/B_S) or high reset properties. (These techniques have been previously effective in reducing unbalance.)

In reviewing the general nature of the causes and effects of LIVC unbalance, transformer core unbalance (occurring only in normally nonsaturated cores) is defined as "the ratcheting or shifting of the minor B-H loop from normal zero centering to one end of the major B-H loop". The shifting of the minor B-H loop is caused by unequal volt-second integrals applied in opposite directions during succeeding half-cycles of operation. Generally, if LIVC unbalance occurs, it is

- Caused by a mismatch of LIVC oscillator transistors,

- Manifested initially as a core unbalance in the current feedback transformer core,
- Observed as an unbalance in the power transformer due to an unbalance in the current feedback transformer,
- Most significant when it results in severe unbalance in the power transformer core while the LIVC is operating from a low impedance source.

Usually, a transistor mismatch affects the core balance in the current feedback transformer rather than in the power transformer because transistor emitter-base voltages are the only factors determining the voltages on the current feedback transformer. Transistor emitter-collector voltages subtract only a small percentage from the LIVC input voltage, with the difference during each half-cycle determining the volts per turn on the power transformer. However, unbalance in the power transformer is often a direct cause of current feedback transformer unbalance. Power transformer unbalance is caused by succeeding half cycles of unequal time durations which result from 1) the end of a "short half cycle" caused by current feedback transformer core saturation rather than the switching inductor, and 2) the end of a succeeding "long half cycle" caused by the switching inductor. While the voltages applied to the power transformer may be equal in this "short-long half cycle" condition, unequal times result in the application of unequal volt-second integrals. A severe unbalance in the power transformer results from a periodic saturation in one direction which causes the LIVC input impedance to be very low at that time. If the LIVC is operating from a low impedance source, high input current spikes will be drawn periodically from the source, resulting in decreased efficiency and increased component stress. If the LIVC is operating from a high impedance source such as a radioisotope thermoelectric generator, the problem is decreased because the source limits the LIVC input current, while the resistive characteristic of the source tends to decrease the occurrence of the unbalance itself.

The matching of power transistors, especially for $V_{BE(SAT)}$, has proven to be an effective method of decreasing unbalance in transformer core drive. The use of cores with high reset properties for LIVC transformers has been effective in reducing the degree of core unbalance resulting from residual core drive unbalance (imperfect transistor matching). The approach discussed in paragraphs a and b below complements these methods and provides a means of compensating for imperfections in transistor matching and any mismatches which may occur as a result of temperature changes, aging, or exposure to nuclear radiation.

a. Circuit Operation - The circuit shown in Figure 9 is a closed loop system which efficiently equalizes the volts per turn on the current feedback transformer during succeeding half cycles. The closed loop operation involves:

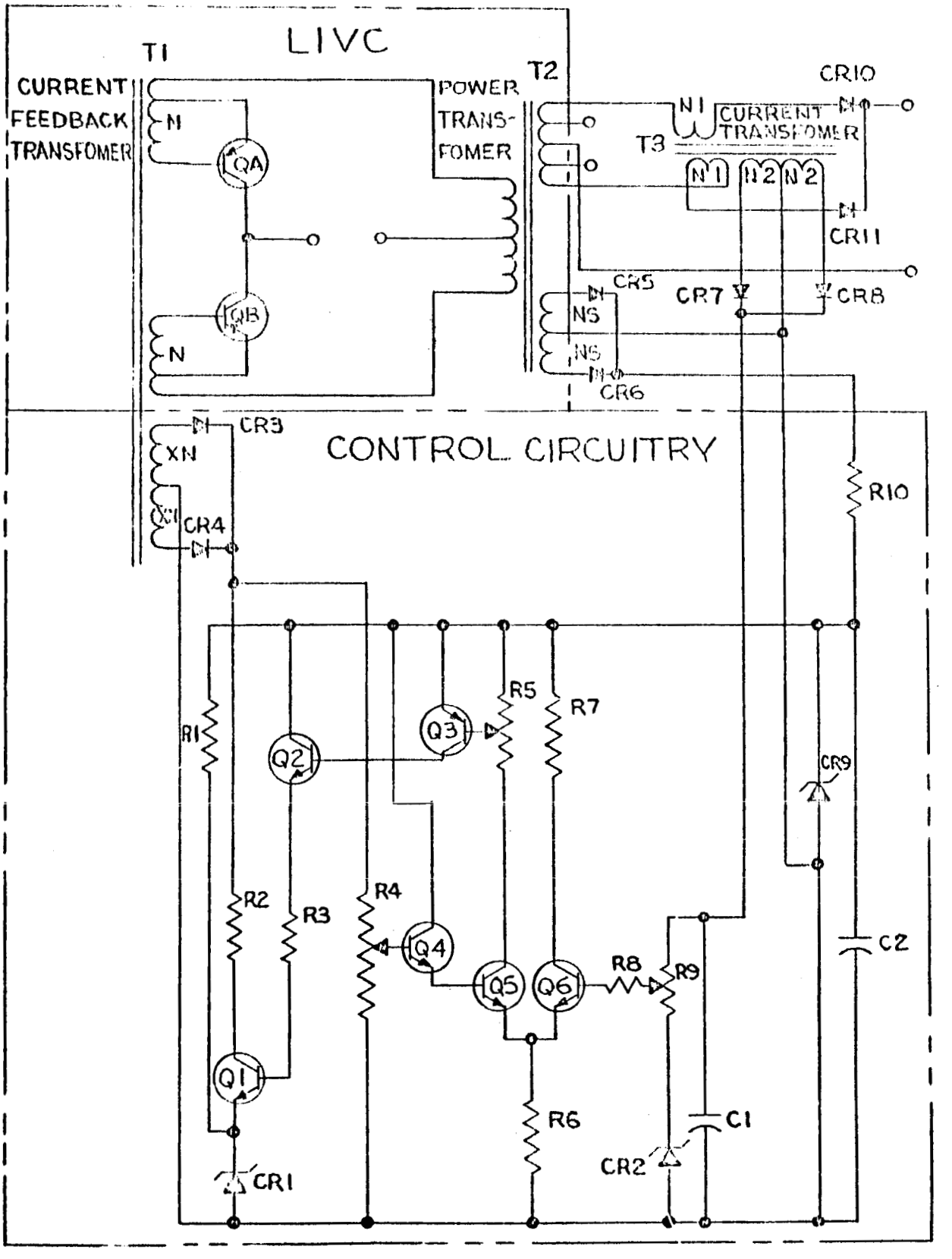
1) Sensing the volts per turn on the current feedback transformer determined by the emitter-base voltage of the conducting LIVC power transistor,

2) Comparing the sensed voltage to a reference voltage which is proportional to load current, and

3) Subtracting drive current from the slightly overdriven LIVC power transistors so the sampled voltage equals the reference voltage.

The fixed amp-turn input (for a specific LIVC input current) to the current feedback transformer and the resistive characteristics of power transistor emitter-base junctions are inherent circuit properties used to an advantage in achieving the control discussed.

The volts per turn (proportional to the emitter-base voltage of QA and QB) on the current feedback transformer T1 is sensed by the multi-turn winding XN and applied across R4 during each half cycle through CR3 or CR4. The

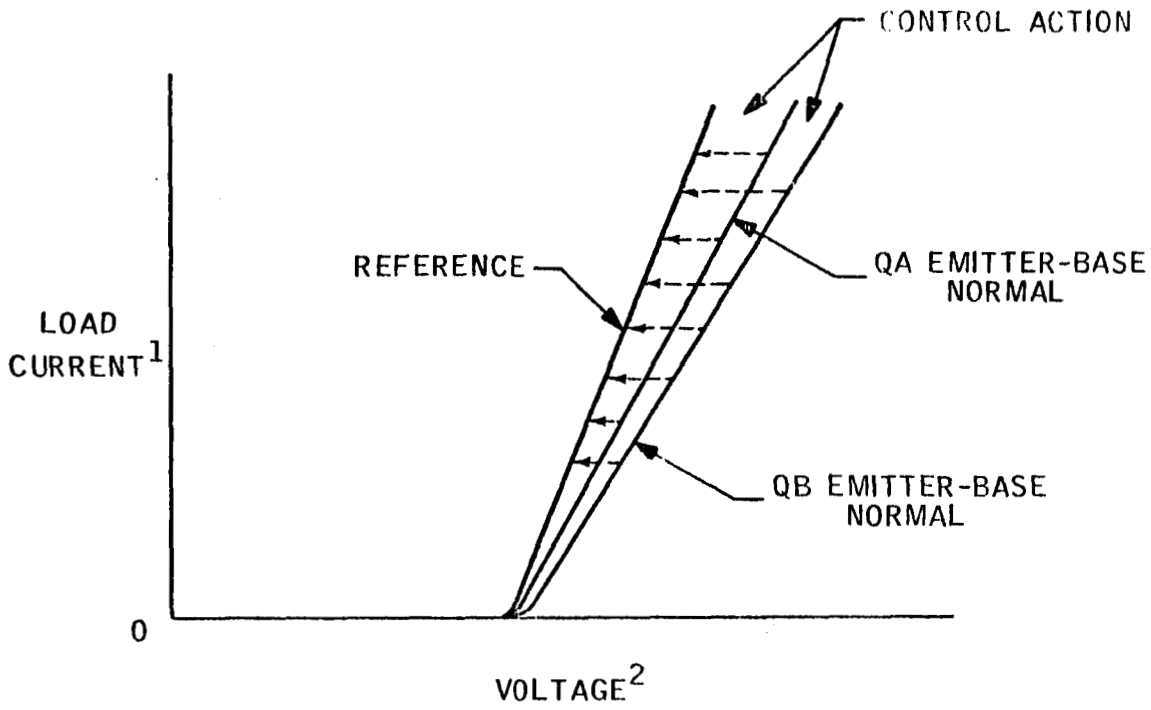

LIVC
T1
CURRENT FEEDBACK TRANSFOMER
N
QA
QB
N
T2
POWER TRANS-FOMER
CR10
N1
CURRENT TRANSFOMER
T3
N1
N2
N2
CR11
CR5
CR7
CR8
NS
NS
CR6
CONTROL CIRCUITRY
CR3
XN
X1
CR4
R10
R1
Q2
Q3
R5
R7
CR9
R2
R3
R4
Q4
Q5
Q6
R8
R9
C2
Q1
R6
C1
CR2
CR1

The voltage reference is established through current transformer T3, CR7 and CR8, R9, CR2, and C1. Current flowing through winding N2 of T3 is directly proportional to load current; therefore, the voltage developed across the parallel combination of R9 in series with CR2 and C1 is proportional to load current. (See Figure 10.)

The emitter-base current and voltage for QA or QB is also proportional to load current. (An initial non-linearity in the emitter-base voltage is matched by CR2 in the reference.) Although both the emitter-base voltage and the reference voltage are proportional to load current, the reference voltage is proportional to the average load current during successive half cycles (C1 provides averaging); the emitter-base voltage is proportional to the load current flowing during that particular half cycle (through CR10 or CR11).

The comparison of the voltage on the current feedback transformer during a particular half cycle to the reference voltage is provided by the differential amplifier consisting of Q5, Q6, R5, R6 and R7. Impedance matching is provided by Q4 and R8. The voltage at the R4 wiper will normally be higher than that at the R9 wiper before any closed loop control is introduced because QA and QB are purposely overdriven initially. The differential amplifier output is amplified by Q3 and Q2 and introduced to Q1.

Drive current is subtracted from QA or QB by causing current to flow out of winding XN of T1, through CR3 or CR4, through R2, Q1, and CR1 back to the XN center tap. (CR1 facilitates control by raising the emitter of Q1 above ground.) If a mismatch occurs between QA and QB, more current is subtracted from either QA or QB by causing current to flow out of winding XN of T1, through CR3 or CR4, through R2, Q1 and CR1 back to the XN center tap. (CR1 facilitates control by raising the emitter of Q1 above ground.) If a mismatch occurs between QA and QB, more current is subtracted during one half of a cycle than during the other. As shown in Figure 10, current is



1 LOAD CURRENT REFERS TO AVERAGE FOR REFERENCE AND SPECIFIC HALF-CYCLE FLOW FOR QA AND QB

2 REPRESENTS MULTIPLE OF ACTUAL VOLTAGES DEVELOPED ACROSS R4 AND R9 (SEE FIGURE 9).

Figure 10 - COMPARISON OF REFERENCE VOLTAGE AND POWER TRANSISTOR EMITTER-BASE VOLTAGES

subtracted on each half cycle by an amount which causes the voltage on the emitter-base junction of the conducting transistor to be equal to a multiple of the reference voltage. The example of Figure 10 shows QB with a higher emitter-base impedance than QA; therefore, more drive current will be subtracted from QB than QA. Amp turns of drive current are subtracted at a high turns-to-ampere ratio through winding XN, resulting in very little power loss. The fact that QA and QB are initially over-driven allows drive currents to be subtracted (decreased current gain) without significant changes in emitter-to-collector voltages.

The bias supply for the circuit is provided by winding N3 of T2, CR5, CR6, R10, CR9 and C2. Therefore, the current subtracted through winding XN of T1 includes only the very low current through R4 which provides sensing, and the current through R2 which does the actual controlling.

Assuming that the LIVC has been operating so that bias power and a reference voltage is established, control during a half cycle of operation when QA conducts consists of the following steps:

1) QA begins to conduct,

2) CR3 conducts and a multiple of the QA emitter-base voltage is applied across R4,

3) R4 voltage initially exceeds R9 voltage; Q5 conducts more current,

4) Q3 and Q2 drive Q1 harder so amp-turns are subtracted from T1 through winding XN, CR3, R2, Q1 and CR1,

5) The stable operating point is achieved when the number of amp-turns subtracted through XN result in an equalization of voltages across R4 and R9.

The operation during the succeeding half-cycle with QB conducting is identical, except that current flows from XN through CR4.

Laboratory testing of this circuit approach has shown that equal volts per turn on the current feedback transformer during succeeding half-cycles could be achieved efficiently even with a 25% mismatch in power transistors. The initial laboratory work indicated that trimming of various circuit components could possibly result in even better performance. Descriptions of additional work and more conclusive laboratory data will be presented in succeeding reports.

b. Circuit Advantages and Limitations - The basic concept of driving the LIVC power transistors to unequal forced current gains to effect equal emitter-base voltages has been utilized successfully in the past. This was accomplished by physically varying the number of drive windings on a particular transistor to match the emitter-base voltages at a specific operating point. The closed loop circuit approach (Figure 9), provides a considerable advantage by achieving matching, not only at one specific point, but throughout load and temperature ranges, and also under the effects of aging and exposure on junction voltage characteristics. Control is achieved with negligible power dissipation because no series elements are added in high current paths, because the ampere-turns of drive are subtracted at a high turns-to-ampere ratio, and because the reference voltage for the closed loop control is varied in proportion to the load, thereby minimizing the degree of control necessary over the load range. An additional significant advantage is that all bias power is supplied by the power transformer; therefore, except for the small current necessary for sensing, the only amp-turns subtracted from the current feedback transformer are those actually providing the desired control.

However, the circuit requires additional components; therefore, the value of the control provided must be compared to the cost of added circuitry for a specific application. The degree of power transistor mismatch which can be compensated is limited by current flowing in the power transformer emitter-base junction and its resistance characteristics. For example, if the transistor mismatch is great and the current level low, the control circuit could turn the oscillator off by subtracting too much drive before equal voltages are achieved. For this reason, the circuit approach is meant to complement, rather than replace, the procedure of initially matching transistors and using high reset cores.

The circuit approach will be especially advantageous in high current systems with long mission times. The approach is especially well suited to high current systems because of its efficient means of control and the latitude of control provided by the high current characteristics. Transistor characteristics would be most likely to change (possibly unequally) on a long mission; closed loop control in this application would be especially advantageous.

II. NEW TECHNOLOGY

The new technology developed this quarter involves each of the three general work areas described in the Technical Discussion (section I. C).

The automatic failure sensing and compensation circuit (section I. C. 1) for the PWM regulator drive and control is a significant step toward the development of a redundant LIVCR with failure correction features.

The circuit to synchronize four redundant LIVCs out of phase (section I. C. 2.) appears to be most applicable to the high power, high reliability systems required for future space missions. Transient reduction and increased reliability features are the primary advantages of this circuit.

Closed loop control of voltages on the LIVC current feedback transformer (section I. C. 3.) appears to be quite effective in maintaining equal transformer core drive during succeeding half cycles, even when a mismatch occurs in LIVC power transistors. Closed loop control could be especially useful in reducing half cycle unbalance on extended space mission applications, where changes in transistor parameters could reasonably be expected.

III. PROGRAM FOR THE NEXT QUARTER

The work planned for the next quarter will include:

1) Development of automatic failure sensing and compensation circuitry for the PWM regulator power sections,

2) Additional refinement and testing of the circuit to decrease unbalance in the LIVC current feedback transformer, and

3) Battery charging studies involving the charge of third electrode batteries with the basic LIVCR circuit.

A primary task in the development of the failure correction circuitry will be the evaluation of various elements which can be used to isolate or introduce various power sections. The additional design work on the circuit to decrease unbalance will lead to a more conclusive evaluation of its merits as an effective element in a power conditioning system. Battery charging studies will be directed toward achieving a more versatile LIVCR, as a power conditioning block in the power system.

IV. CONCLUSIONS AND RECOMMENDATIONS

A. FAILURE SENSING AND COMPENSATION CIRCUITRY

The automatic failure sensing and compensation circuitry developed (and successfully tested) for the redundant PWM drive and control circuits during this quarter have resulted in the following conclusions and recommendations:

1) All drive and control circuit failures are indicated by one of the following combinations of regulator operational characteristics.

   - The regulator output voltage is too high and drive current is supplied to the regulating transistor.
   - The regulator output voltage is too low and no drive is supplied to the regulating transistor.

2) Total PWM transistor drive current, rather than a percentage, shall be sensed at some point in the amplification circuit.

3) The switch reliability necessary for connecting and isolating the circuits can be achieved with a rigidly specified transistor operating at a fraction of its rating.

4) The latch-up provision, depending on the conditions of redundant circuits, is desirable to assure positive transition from one circuit to another.

5) A non-destructive switch is required for this application because the switch may be required to function more than once.

6) An integrated circuit could replace functional blocks in the operational unit. This approach is especially recommended for space applications where size, weight and reliability are critical.

B. SYNCHRONIZATION OF FOUR LIVCs WITH PHASE SEPARATIONS OF 45 DEGREES

The circuit which synchronizes four LIVCs at 45-degree phase separations appears especially well suited for incorporation in high power, high reliability power systems. This circuit has the following performance characteristics:

1) Frequency is directly proportional to the LIVC input voltage.

2) Phase separated synchronization is established reliably upon applying a starting pulse to any combination of LIVCs.

3) Phase separated synchronization is maintained without significant frequency change even after failures in individual LIVCs of the redundant combination.

C. SYNCHRONIZATION OF FOUR LIVCs WITH PHASE SEPARATIONS OF 120 DEGREES AND 0 DEGREE

The circuit which synchronizes four LIVCs at 120-degree phase separations (two LIVCs are in phase) requires additional design work to ensure acceptable performance during start-up and after failures. Because of the indicated superiority of the synchronization circuit described in paragraph B above, additional work on this approach is not recommended.

D. DECREASING UNBALANCE IN THE LIVC CURRENT FEEDBACK TRANSFORMER

The circuit approach to decrease unbalance in the LIVC current feedback transformer has provided favorable results in initial laboratory testing. This circuit requires additional work to optimize the design and to more conclusively evaluate its merit as a system component. The following conclusions and recommendations are based on initial investigations of this circuit:

1) The circuit approach equalized the electrical drive (power transistor emitter-base voltages) applied to the transformer core during succeeding half-cyles even when a mismatch exists between LIVC power transistors. This feature decreases unbalance by removing one basic cause of unbalance.

2) The circuit is limited in the amount of LIVC power transistor mismatch it can compensate.

3) The circuit is recommended as a complement to matched power transistors and high reset transformer cores for decreasing unbalance.

4) The load-variable reference provided with the closed loop control is basic to efficient operation of the circuit.

5) The high turns-to-ampere ratio with which ampere-turns are subtracted from the current feedback transformer is instrumental in achieving efficient operation.

6) The LIVC power transistors should be initially overdriven if closed loop control is introduced.

7) The circuit bias power supplied by the LIVC power transformer is significant in effecting accurate closed loop control and in ensuring that the introduced circuit produces no interference when the LIVC starts.

8) The circuit approach seems especially well suited to systems with high reliability requirements in which transistor parameter changes can be reasonably expected. Transistor changes can be caused by load and temperature changes, aging or exposure to nuclear radiation.

9) The added complexity of the circuit approach must be justified by favorable results in future performance evaluations.